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FOR

SPREAD-SPECTRUM RECEIVERS WITH EXTENDED DYNAMIC RANGE

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SPREAD-SPECTRUM RECEIVERS WITH EXTENDED DYNAMIC RANGE

Field of the Invention

The present invention relates to signal processing, and, in particular, to receivers for spread-spectrum signals.

Background of the Invention

Fig. 1 shows a high-level block diagram of a conventional spread-spectrum receiver **100** of the prior art. Those skilled in the art will understand that certain elements such as filters, amplifiers, attenuators, oscillators, synthesizers, and the like have been omitted from this figure, as well as from other figures of receivers in this application.

As indicated in Fig. 1, receiver **100** receives a radio frequency (RF) spread-spectrum input signal **102** from an antenna. Mixer **104** downconverts input signal **102** from RF to an intermediate frequency (IF) using RF-to-IF mixing signal **106** to form IF signal **108**. Analog-to-digital converter (ADC) **118** converts analog IF signal **108** into a digital IF signal **120**. Using IF-to-baseband mixing signal **122**, digital downconverter **124** downconverts IF signal **120** into a baseband signal **126**. Digital (e.g., low-pass) filter **128** filters baseband signal **126**, e.g., to filter out undesirable interference from other signals, to generate filtered signal **130**, which is then subjected to further digital processing **132** (e.g., de-spreading / demodulation) to generate digital incoming data signal **134**.

In a typical spread-spectrum receiver, such as receiver **100**, errors can result from such phenomena as thermal noise from analog processing prior to the A/D conversion, non-coherent on-channel interference, and off-channel interference. It is assumed that digital filter **128** has a sufficient number of taps to reject off-channel interference prior to demodulation and provide a desired signal level above sensitivity to digital processing **132**. Under these conditions, the level of interference that can be tolerated at the A/D conversion step is determined by the thermal noise and the dynamic range of ADC **118**. Here, dynamic range is defined as the difference in dB between the full-scale ADC input level and the quantization-noise floor level, where the quantization-noise floor level is determined by the least significant bit (LSB) of the ADC.

The ADC dynamic range *DR* for first Nyquist zone sampling can be expressed by Equation (1) as follows:

$$DR\ (\text{dB}) = 6*N + 1.76 + 10*\log\ (BW_N/BW_S), \qquad (1)$$

where N is the number of effective bits in the ADC (i.e., typically one fewer than the total number of bits), BW_N is the Nyquist bandwidth (i.e., one-half the sample clock frequency), and BW_S is the desired

signal bandwidth. For a 14-bit ADC (with 13 effective bits) operating with a 61.44-MHz sample clock and a 3.84-MHz wide UMTS signal bandwidth, the dynamic range *DR* is 88.8dB. In practice, sampling is performed at higher Nyquist zones, where there are additional noise contributions that reduce the dynamic range somewhat.

Fig. 2 shows a graphical representation of the relative levels of thermal noise, quantization noise, and a desired signal level for a 14-bit ADC receiving a UMTS signal at a signal-to-thermal-noise ratio (SN_tR) of 0dB, where the SN_tR is proportional to the log of (signal power / thermal noise power). As indicated in Fig. 2, for 10dB of thermal noise, 78.8dB of ADC headroom is provided, where ADC headroom is defined as the difference in dB between the full-scale ADC input level and a specified desired signal level (in this case, at 18dB above sensitivity).

Fig. 3 shows a graphical representation of the relative signal and noise levels for the same 14-bit ADC when 75dB of off-channel interference is introduced into the receiver above the desired signal level. Because the 14-bit ADC has 78.8dB of headroom, this relatively large off-channel interference can be tolerated without overflowing the ADC. It is assumed that the off-channel interference can be sufficiently removed by digital filter **128** after the A/D conversion to enable satisfactory digital processing **132**.

Fig. 4 shows a graphical representation of the relative signal and noise levels when receiver **100** is implemented using a 12-bit ADC instead of a 14-bit ADC for an SN_tR of 0dB. According to Equation (1), the ADC dynamic range *DR* is only 76.8dB, and the ADC headroom is only 66.8dB for first Nyquist zone sampling for a 12-bit ADC (with 11 effective bits) operating with a 61.44-MHz sample clock and a 3.84-MHz wide UMTS signal bandwidth.

Fig. 5 shows a graphical representation of the relative signal and noise levels for the 12-bit ADC of Fig. 4, when the same 75dB off-channel interference of Fig. 3 is introduced. Here, the 66.8dB of ADC headroom is insufficient to tolerate such relatively large off-channel interference, and the ADC will overflow, resulting in undesirable data errors downstream.

Brief Description of the Drawings

Aspects, features, and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims, and the accompanying drawings in which like reference numerals identify similar or identical elements.

Fig. 1 shows a high-level block diagram of a conventional spread-spectrum receiver of the prior art;

Fig. 2 shows a graphical representation of the relative signal and noise levels for the receiver of Fig. 1 implemented with a 14-bit ADC and receiving a UMTS signal at an SN_tR of 0dB;

Fig. 3 shows a graphical representation of the relative signal and noise levels for the receiver of Fig. 2 when 75dB of off-channel interference is introduced into the receiver above the desired signal;

Fig. 4 shows a graphical representation of the relative signal and noise levels for the receiver of Fig. 1 implemented with a 12-bit ADC and receiving a UMTS signal at an SN_tR of 0dB;

Fig. 5 shows a graphical representation of the relative signal and noise levels for the receiver of Fig. 4 when the same 75dB off-channel interference is introduced;

Fig. 6 shows a high-level block diagram of a spread-spectrum receiver, according to one embodiment of the present invention;

Fig. 7 shows a block diagram of the variable attenuator and the ADC of Fig. 6, according to one possible implementation of the receiver of Fig. 6;

Fig. 8 shows a graphical representation of the relative signal and noise levels at sensitivity when the receiver of Fig. 6 is implemented using a 12-bit ADC for a UMTS signal having an SN_tR of -18dB; and

Fig. 9 shows a graphical representation of the relative signal and noise levels at 18dB above sensitivity when the receiver of Fig. 8 is implemented using a 12-bit ADC for a UMTS signal having an SN_qR of -10dB, where the 20dB variable attenuator of Fig. 6 is turned on.

Detailed Description

Fig. 6 shows a high-level block diagram of a spread-spectrum receiver **600**, according to one embodiment of the present invention. Receiver **600** is similar to prior-art receiver **100** of Fig. 1, except that receiver **600** also has a variable attenuator **614** that selectively attenuates the incoming signal based on a control signal generated by a controller **612** monitoring the output of ADC **618** (i.e., prior to interference filter **628**).

In particular, receiver **600** receives an RF spread-spectrum input signal **602** from an antenna. Mixer **604** downconverts input signal **602** from RF to IF using RF-to-IF mixing signal **606** to form IF signal **608**. Depending on a control signal **610** from controller **612**, variable attenuator **614** selectively attenuates IF signal **608** to generate an attenuated IF signal **616**. Alternatively, control signal **610** can instruct variable attenuator **614** not to attenuate IF signal **608**. In either case, ADC **618** converts the analog IF signal into a digital IF signal **620**. Using IF-to-baseband mixing signal **622**, digital downconverter **624** downconverts IF signal **620** into a baseband signal **626**. Digital filter **628** filters baseband signal **626** to generate filtered baseband signal **630**, which is then subjected to further digital processing **632** (e.g., de-spreading / demodulation) to generate digital incoming data signal **634**.

In one possible implementation, controller **612** samples and compares the output of ADC **618** to a specified (e.g., programmable) upper threshold level. When the ADC output exceeds the upper threshold, controller **612** turns on variable attenuator **614** via control signal **610**, in which case, the analog signal presented to ADC **618** is an attenuated version of IF signal **608** generated by mixer **604**. Similarly, when the ADC output is less than a specified (e.g., programmable) lower threshold level, controller **612** turns off variable attenuator **614**, in which case, the analog signal presented to ADC **618** is an un-attenuated version of IF signal **608**. In order to avoid having the receiver toggle back and forth repeatedly between attenuation and non-attenuation, the lower threshold level is preferably lower than the upper threshold level by at least the amount of attenuation applied by variable attenuator **614**. In fact, in preferred implementations, hysteresis is achieved by setting the threshold levels such that the difference between the upper and lower thresholds is slightly greater than the applied attenuation. In addition or alternatively, hysteresis can be achieved by requiring the signal level to be higher than the upper threshold or lower than the lower threshold for a specified amount of time before changing the state of the attenuator. In any case, hysteresis can be used to avoid situations in which slight fluctuations in signal level result in undesirably rapid toggling on and off of the attenuator.

Fig. 7 shows a block diagram of variable attenuator **614** and ADC **618** of Fig. 6, according to one possible implementation of receiver **600**. In this particular implementation, ADC **618** is a 12-bit ADC, and variable attenuator has two switches **702** and a 20dB attenuator **704**. Switches **702** are controlled by control signal **610** to either bypass or apply 20dB attenuator **704** to selectively attenuate IF input signal **608**. Note that the size of the attenuator will typically depend on the signal requirements for the particular application.

The design of receiver **600** is based in part on the recognition that a spread-spectrum receiver can operate with received RF signals having negative signal-to-noise ratios (i.e., where the noise level is larger than the desired signal level). Referring again to Fig. 6, since the de-spreading processing of digital processing **632** concentrates the desired signal energy in a bandwidth corresponding to the user symbol rate, a signal having a positive SN_tR can be generated (albeit at a lower data rate) during digital processing **632** even when the signal at ADC **618** has an SN_tR that is small or even negative (albeit not too negative). Since noise and interference are uncorrelated with the de-spreading code applied by digital processing **632**, noise is not concentrated in the reduced signal bandwidth. In a typical spread-spectrum receiver, the limiting noise is either thermal noise (at sensitivity) or non-coherent on-channel interference.

Fig. 8 shows a graphical representation of the relative signal and noise levels at sensitivity when receiver **600** of Fig. 6 is implemented using a 12-bit ADC for a UMTS signal having an SN_tR of -18dB.

Even though the received signal's SN_tR is negative, receiver **600** can successfully operate due to the signal-concentration characteristics of spread-spectrum processing, where the de-spreading process implemented by digital processing **632** results in a positive SN_tR.

Fig. 9 shows a graphical representation of the relative signal and noise levels at 18dB above sensitivity when the receiver of Fig. 8 is implemented using a 12-bit ADC for a UMTS signal having a signal-to-quantization-noise (SN_qR) of -10dB, where 20dB variable attenuator **614** of Fig. 6 is turned on. Here, the 20dB of attenuation reduces the desired signal level such that there is 86.8dB of ADC headroom, which, as shown in Fig. 9, enables the receiver to tolerate the same 75dB interference that was tolerated using the 14-bit ADC of Fig. 3. Without the 20dB of attenuation, the ADC headroom in the receiver of Fig. 9 would be only 66.8dB (see Fig. 5), which is not enough tolerate the 75dB interference without overflowing the A/D converter.

For a particular application, the amount of external attenuation that can be applied is bounded according to Equation (2) as follows:

$$P_{int} - P_{FS} \leq \text{Attenuator Value} \leq SN_qR + 18\text{dB}, \quad (2)$$

where P_{int} is the maximum interference power at the ADC input, P_{FS} is the full-scale input of the ADC, and SN_qR is the minimum signal-to-quantization-noise ratio at the interference test conditions without the presence of interference. In Equation (2), 18dB is the lowest (negative) SN_qR at the ADC input at which the signal can still be demodulated and meet the bit-error rate (BER) requirement for that particular application. In other words, the minimum external attenuation value that can be used is equal to how much the maximum allowable interference exceeds the full-scale ADC input power level prior to switching in the external attenuator. Similarly, the maximum external attenuation value that can be used is equal to 18dB above the SN_qR at the interference test level with no interference and no external attenuation.

As described previously, in a preferred implementation, variable attenuator **614** is turned off when the output of ADC **618** is relatively small and turned on when the ADC output is relatively large. By choosing appropriate threshold and attenuation values, receiver **600** should be sensitive enough to process relatively low desired signal levels in the absence of interference, yet capable of processing relatively high received signal levels, whether or not off-channel interference is present (e.g., high desired signal level with no off-channel interference or low desired signal level with strong off-channel interference). In that case, receiver **600** of the present invention can be implemented using a smaller, less-expensive ADC (in this particular case, 12 bits instead of 14 bits) for the same signal application as prior-art receiver **100** of Fig. 1.

In the example of Figs. 8 and 9, the attenuation value of 20dB is derived as follows. The desired signal level under interference test conditions is 18dB above sensitivity (i.e., 66.8 dB below full scale).

The SN_qR at this level is +10dB. The maximum interference level is 79dB above the desired signal level, so the interference level exceeds the full-scale ADC input by 12.2dB. Based on Equation (2), the attenuation value is bounded as follows:

$$12.2\text{dB} \leq \text{Attenuator Value} \leq 28\text{dB}.$$

Choosing 20dB for the attenuator value provides 8dB of margin between the -10dB SN_qR when the attenuator is switched in and the -18dB SN_qR limit for demodulation of the desired signal with acceptable BER.

The present invention differs from conventional automatic gain control (AGC) applications that attenuate received signals prior to A/D conversion, in that AGC applications generate their feedback control signals by measuring only on-channel desired signal and/or noise power level and not off-channel interference (i.e., when there is no off-channel interference or after any such interference has been removed), while the present invention bases its feedback control signal on the total signal output by the ADC whether or not off-channel interference is present.

Moreover, the goal in AGC applications is to maintain a constant level for the desired signal (e.g., a fixed number of dB below the ADC's full scale. In the present invention, on the other hand, the level of the desired signal is substantially irrelevant as long as it falls somewhere within an acceptable range (which happens to include negative SN_tR or SN_qR levels).

Furthermore, the present invention does not have to distinguish whether a high AGC output level corresponds to a strong desired signal or a strong interference signal. As long as the maximum expected interference-to-carrier ratio is known *a priori* (and as long as the ratio is not too high for a given architecture), a predetermined amount of attenuation can be switched in regardless of what type of signal (desired or interference) is causing the upper threshold to be exceeded.

Note, however, that a receiver could in theory be implemented with conventional AGC control in addition to the attenuation control of the present invention.

In the embodiment of Fig. 6, the controller samples the digital output of the ADC. In one possible implementation, the variable attenuator is turned on before the ADC overflows. For example, the upper threshold level can be selected at some appropriate level below the ADC's full scale level (e.g., within 3dB of saturation). In another implementation, the variable attenuator is not turned on until the ADC actually overflows. In this latter case, instead of or in addition to sampling the ADC digital output signal, the controller can sample a special overflow flag generated by the ADC (see Fig. 7) for use in controlling the operations of the variable attenuator.

Although the present invention has been described in the context of a receiver having a 12-bit ADC (with 11 effective bits) operating with a 61.44-MHz sample clock and a 3.84-MHz wide UMTS signal bandwidth, the invention can also be implemented in other contexts having different signals with

different bandwidths, different sample clocks, and/or different ADCs. In general, the present invention can be implemented for any appropriate type of spread-spectrum communication system.

Although the present invention has been described in the context of a variable attenuator that selectively switches in or out a single, fixed amount of attenuation, other variable attenuation schemes can be implemented including gradually switching in multiple, fixed amounts of attenuation at different signal levels or even levels of attenuation that vary smoothly with signal level.

Although the present invention has been described in the context of receiver **600** of Fig. 6, which first converts from RF to IF, then attenuates, then digitizes, then converts from IF to baseband, then filters, and then de-spreads, the invention is not so limited. The present invention can also be implemented in the context of other types of receivers having different architectures. For example, the attenuation and even the digitization could be applied to the RF signal prior to conversion to IF, and/or the filtering and even the de-spreading could be implemented at IF prior to conversion to baseband. Moreover, the conversion from RF to baseband could be implemented in a single step, in either the analog or digital domain, without generating an intermediate IF signal.

Embodiments of the present invention may be implemented as circuit-based processes, including possible implementation on a single integrated circuit (such as an ASIC or an FPGA), a multi-chip module, a single card, or a multi-card circuit pack. As would be apparent to one skilled in the art, various functions of circuit elements may also be implemented as processing steps in a software program. Such software may be employed in, for example, a digital signal processor, micro-controller, or general-purpose computer.

It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be made by those skilled in the art without departing from the scope of the invention as expressed in the following claims.